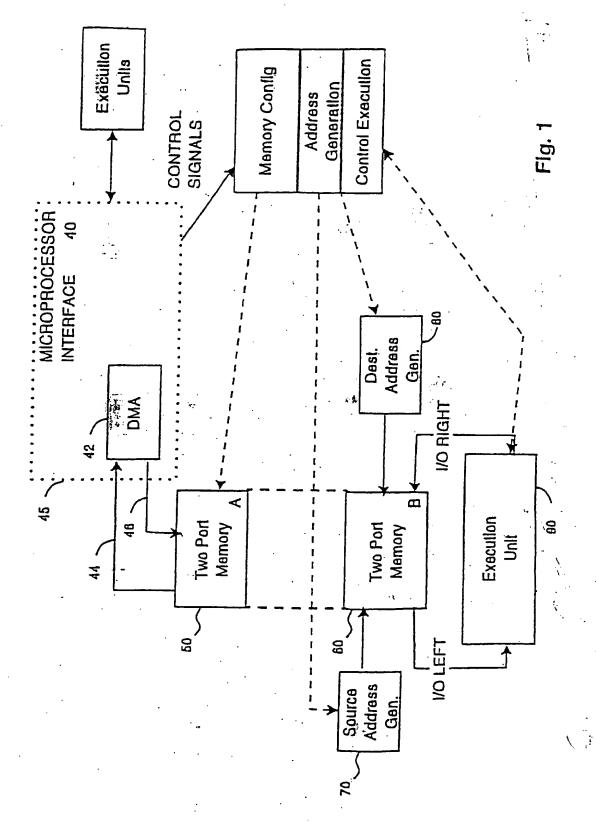


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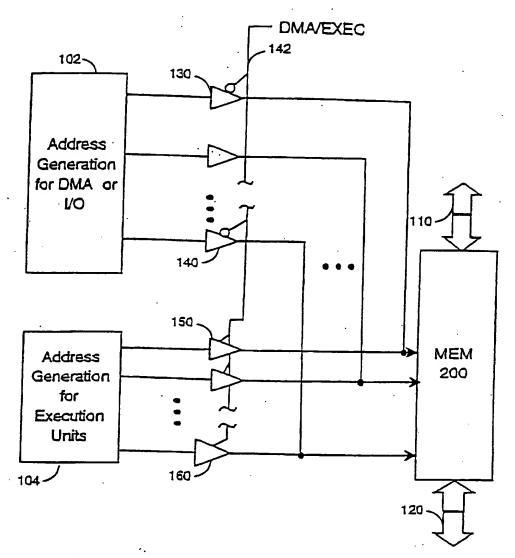


FIG. 2

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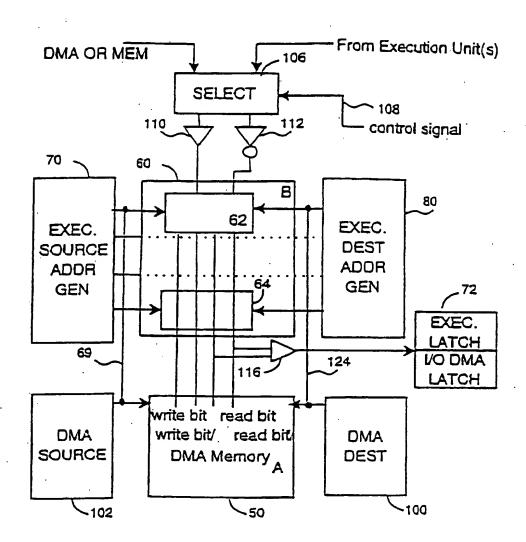
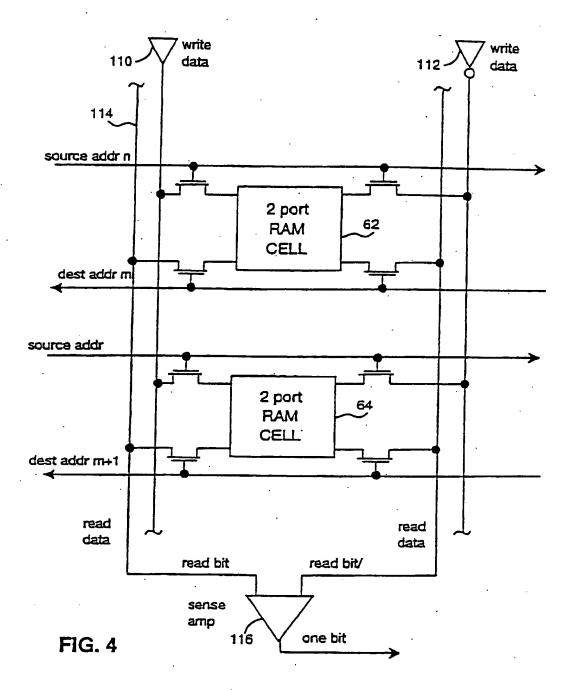


Fig. 3

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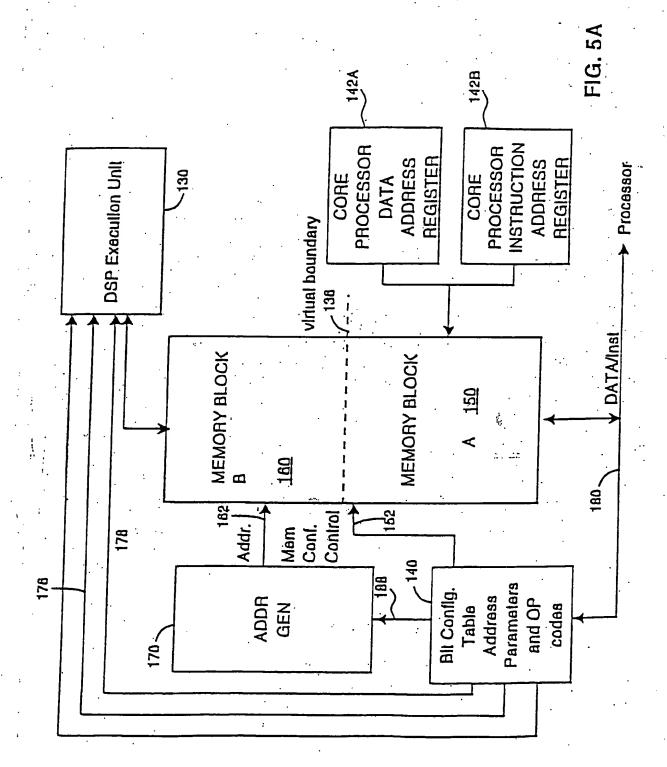
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For: A Tightly Coupled and Scalable Memory and Execution Unit Architecture

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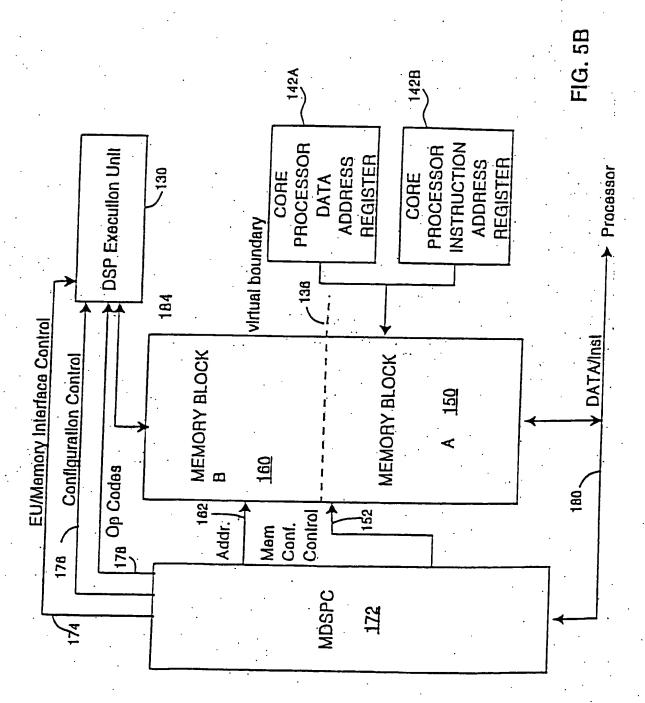
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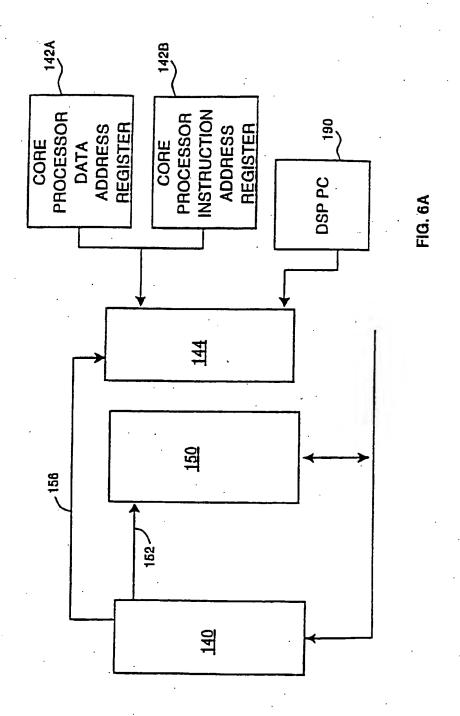
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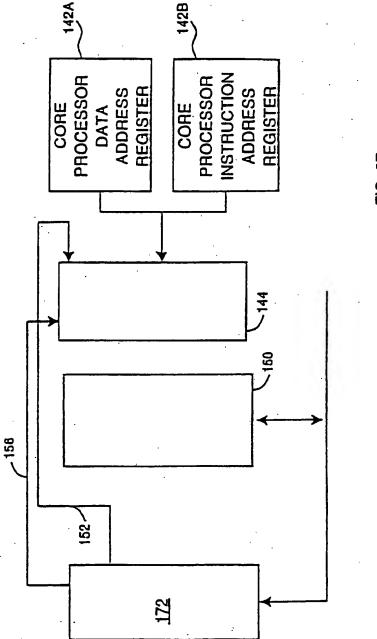


FIG. 6B

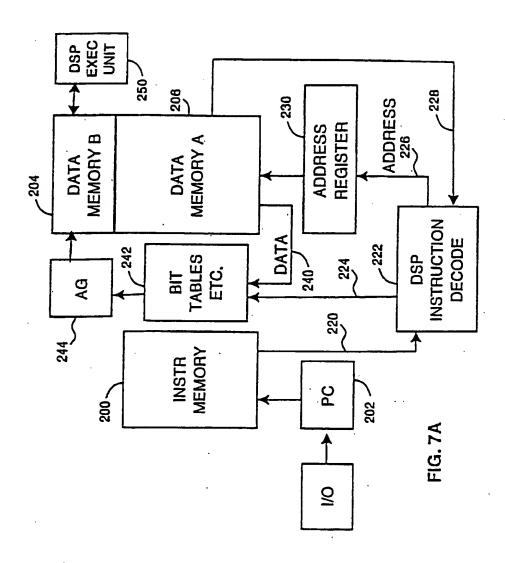


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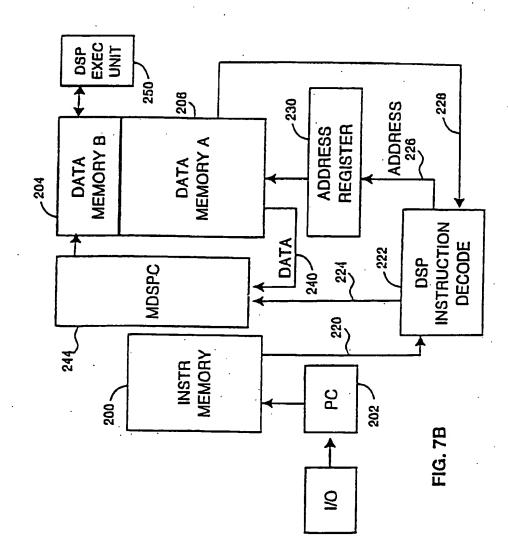
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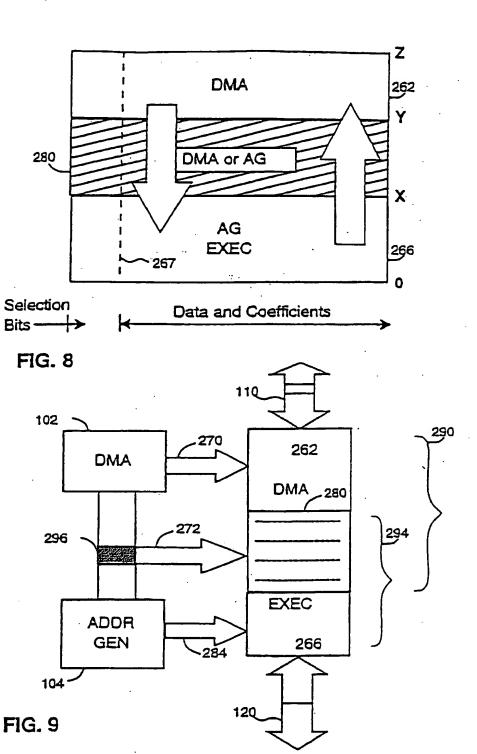
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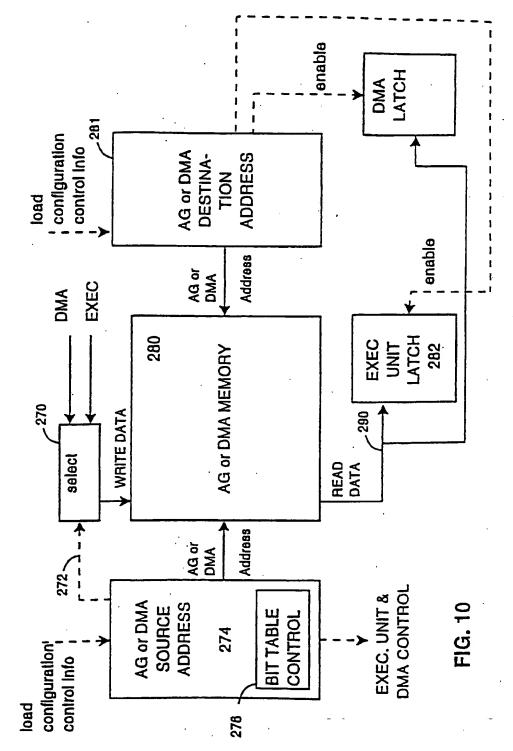
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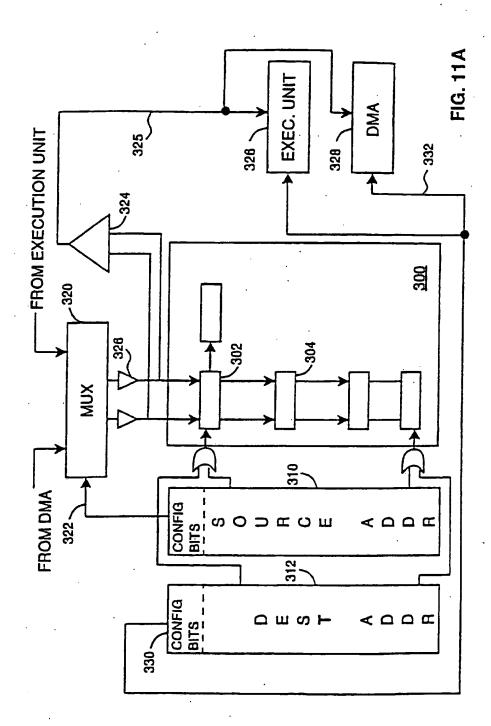
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DEST. DMA **T**5 DMA selection DEST. EXEC exec. selection dest. address read control SOURCE EXEC SOURCE EXEC wrlte
control
exec
selection
address
iatch generator address SOURCE DMA ADDRESS & CONTROL GENERATION MEMORY ACTIVITY

FIG. 11B



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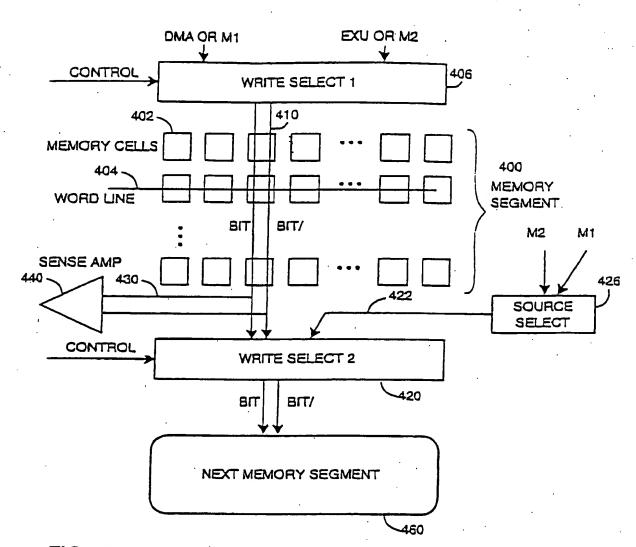
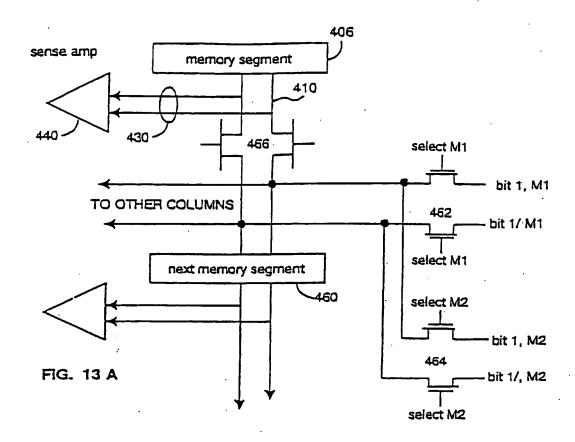
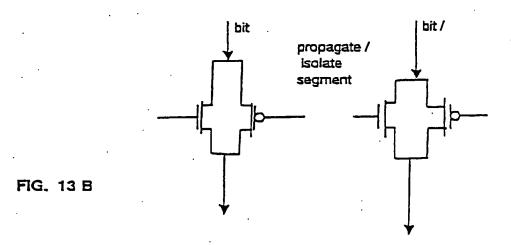


FIG. 12



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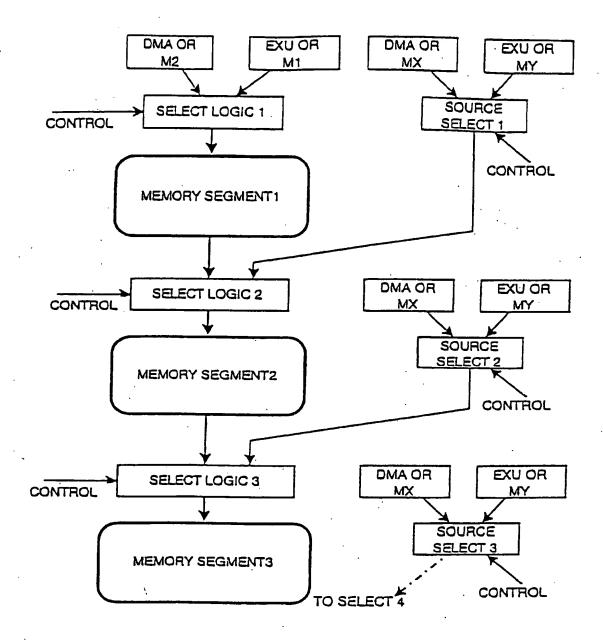


FIG. 14



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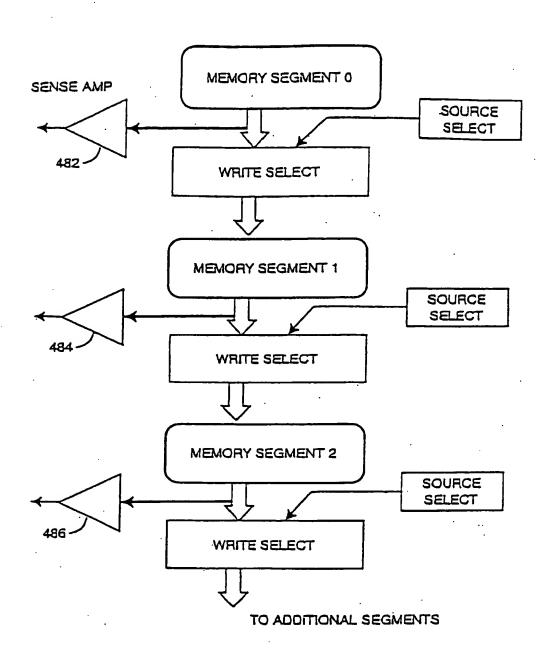
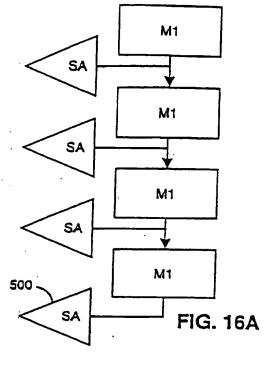
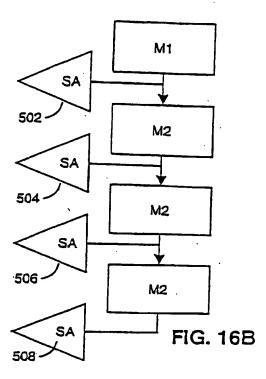


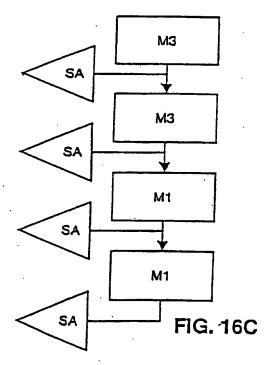
FIG. 15

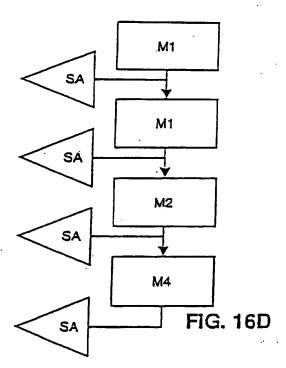
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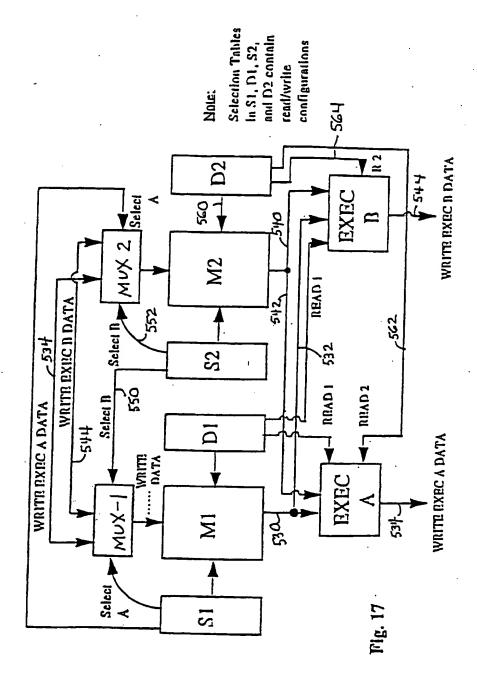
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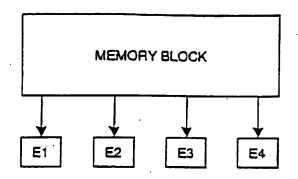


FIG. 18A

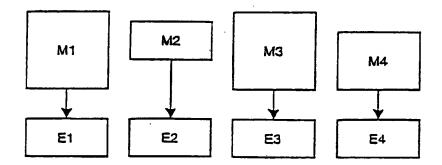


FIG. 18B

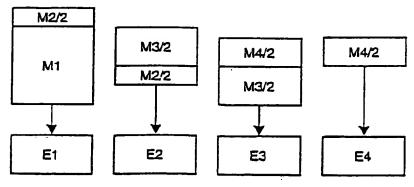


FIG. 18C



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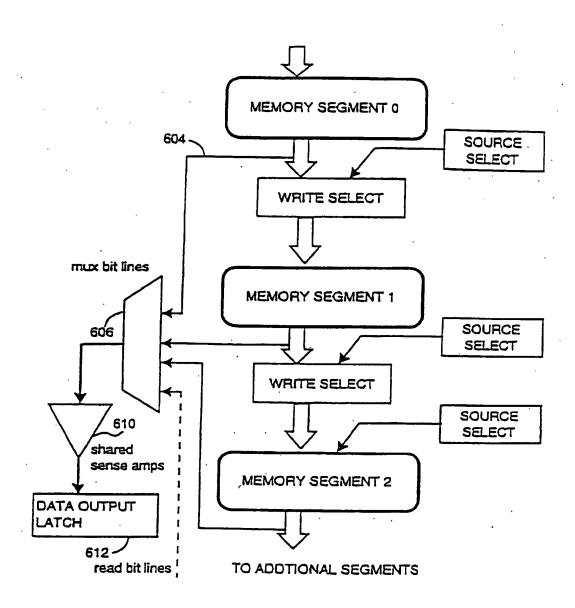


FIG. 19



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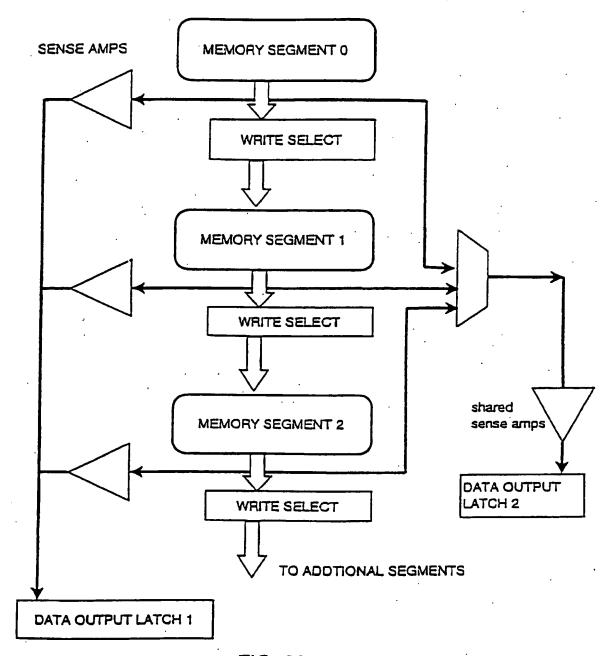
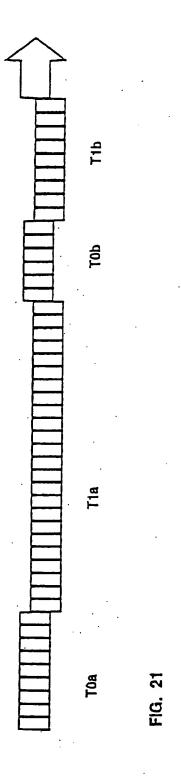


FIG. 20

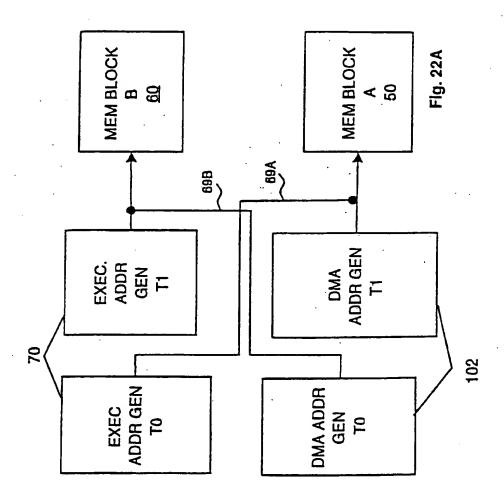


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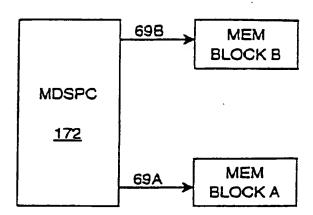


FIG. 22B

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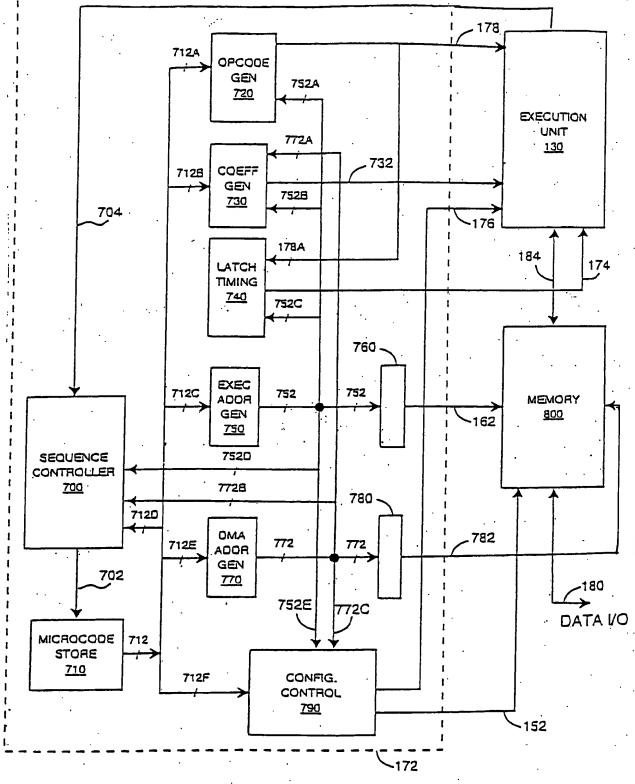


FIG. 23A



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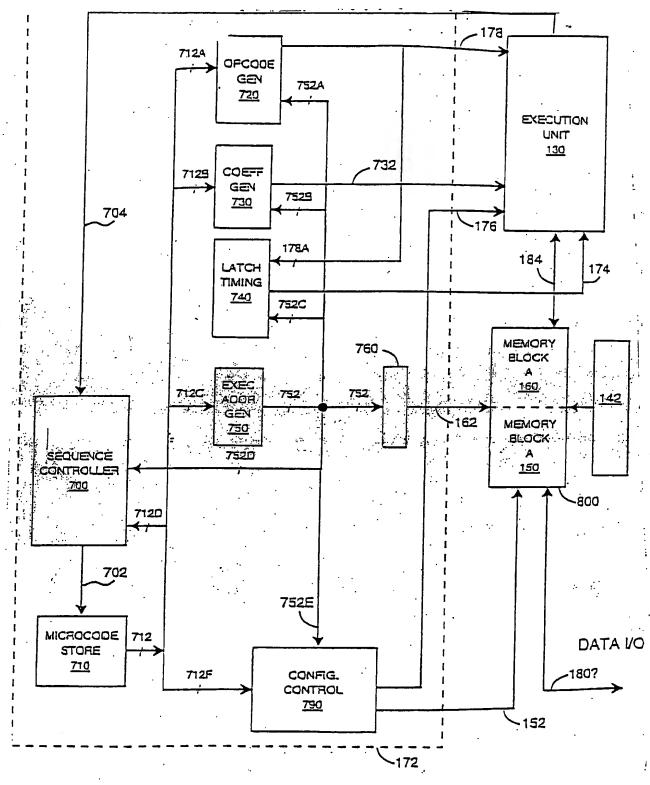


FIG. 23B



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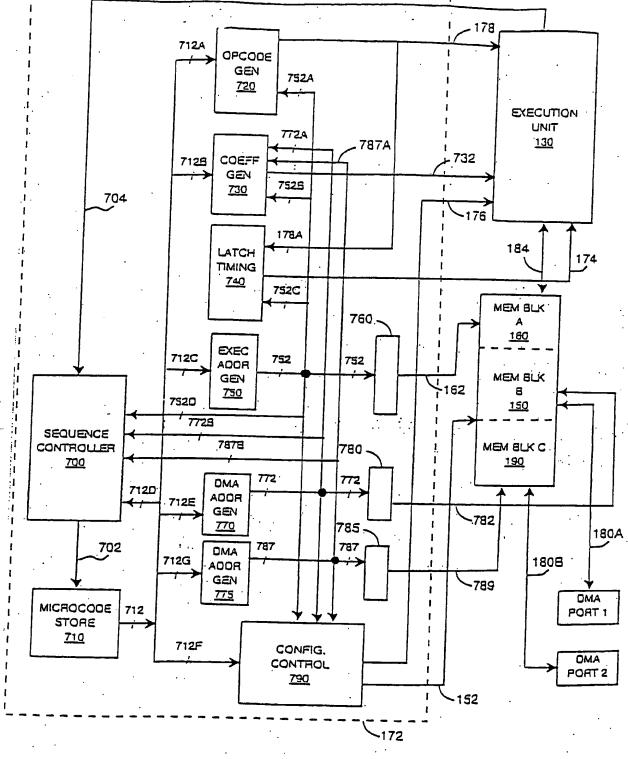


FIG. 23C



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	ADORESS	FUNCTION
	0×710	FFT RADIX 2
	0x905	FIR FILTER
	0x2100	CONVOLUTION
L		

FIG. 24A

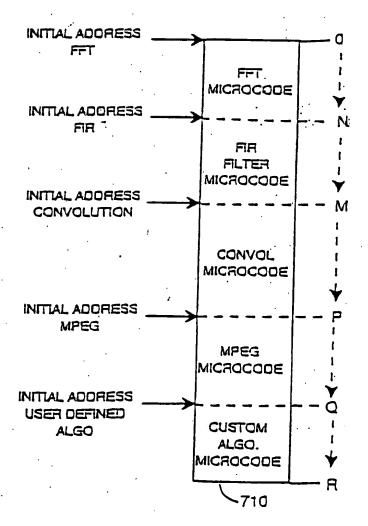


FIG. 24B



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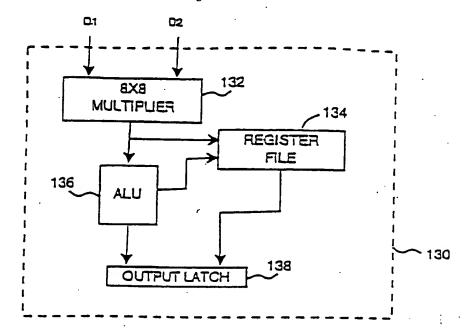


FIG. 25

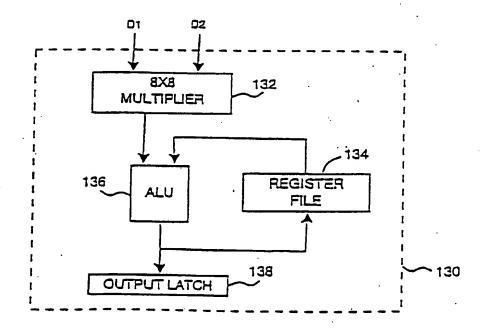
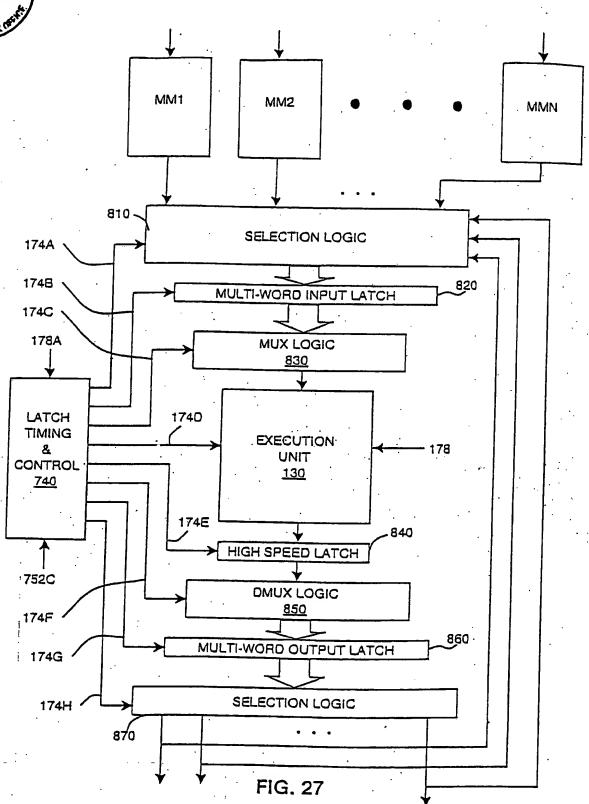


FIG. 26

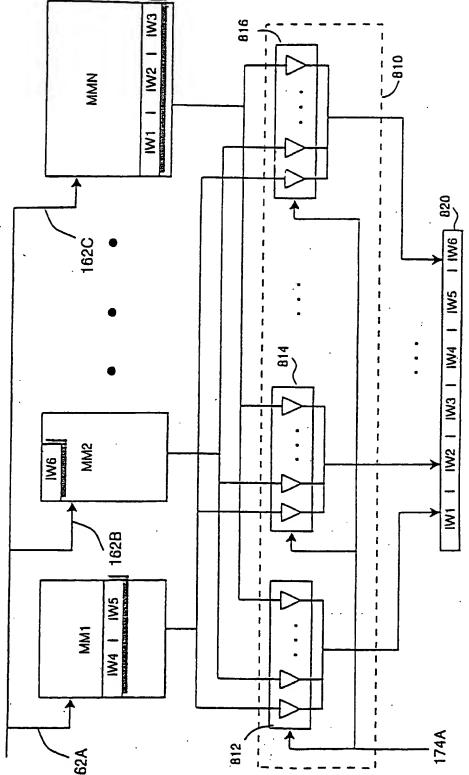
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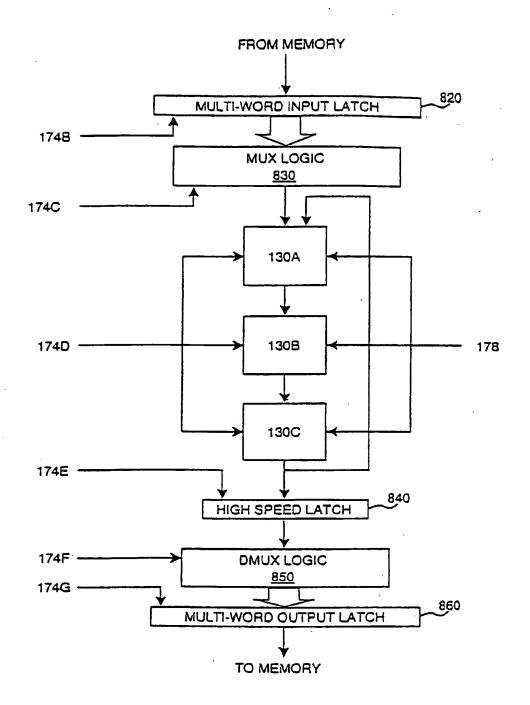
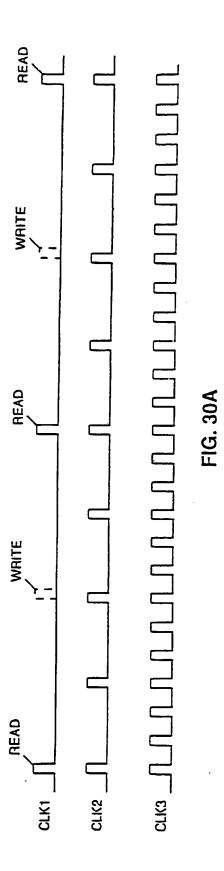
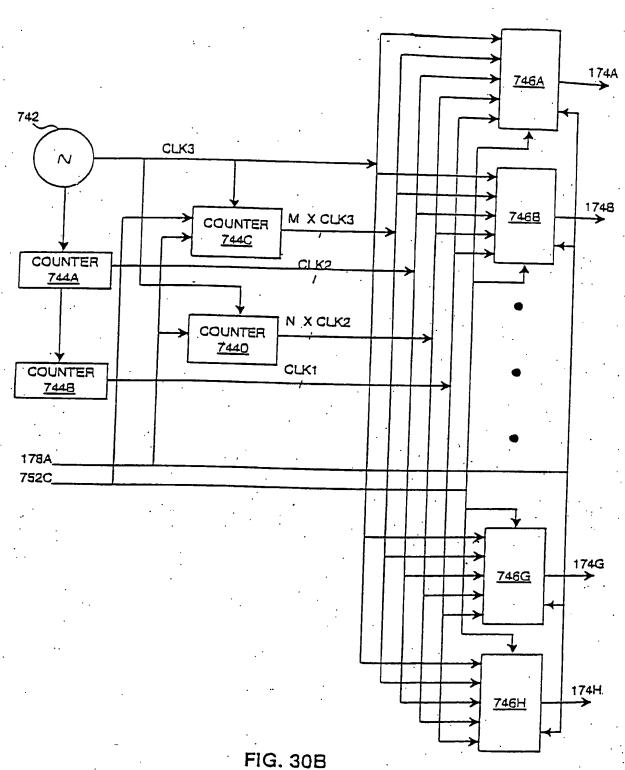


FIG. 29





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MUX LOGIC
830

130A

130B

130C

MULTI-PORTED
REGISTER FILE

FIG. 31

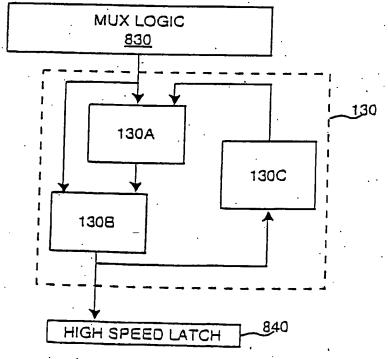


FIG. 32



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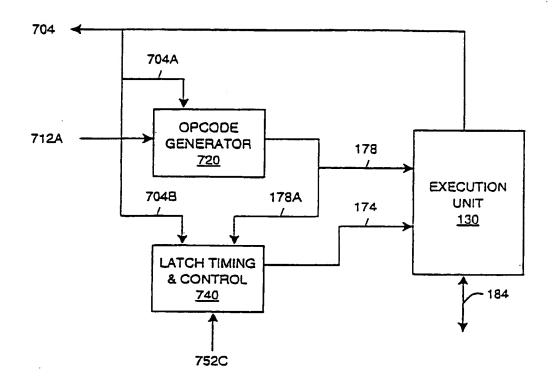


FIG. 33



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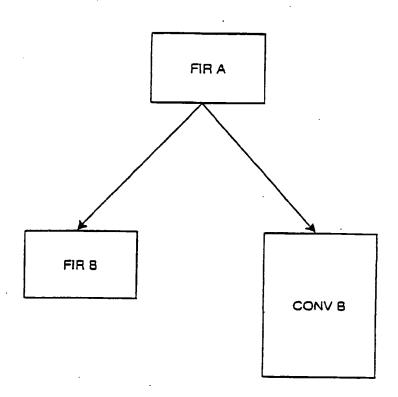


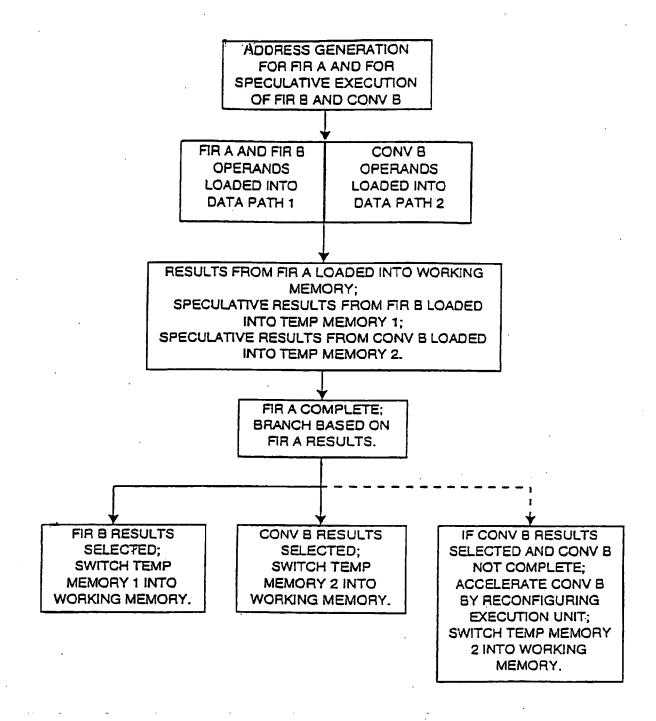
FIG. 34



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WORKING MEMORY	
	
I TEMP MEMORY 1	; ;
TEMP MEMORY 2	 ! !
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TEMP MEMORY N	i
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FIG. 36